CLAIMS

1. Method to detect a sluggishness or the blocking of an electric drive (3), which is triggered via a power semiconductor component (7) and the electric drive (3) can be operated in a partial load range (PWM < 100%) and in a full load range (PWM = 100%) as a function of the timing of a PWM signal (29, 31) and an evaluation circuit (37) is connected with a micro-controller (25), characterized in that pulses generated within a time interval are detected in the evaluation circuit (37) from the current I flowing over the first power semiconductor component (7) and the number of detected pulses A1*, A2* are compared with the to-be-expected number of pulses A1, A2.

2. Method according to Claim 1, characterized in that the currents I flowing in accordance with the PWM signal (29, 31) with each switching through of the first power semiconductor component (7) generate pulses that can be evaluated, which are supplied via taps (11, 12) to the evaluation circuit (37).

3. Method according to Claim 2, characterized in that the number of pulses A1*, A2* supplied to the evaluation circuit (37) is compared with a to-be-expected number of pulses A1, A2.

4. Method according to Claim 2, characterized in that pulses detected by the taps (11, 12) are supplied to a comparator component (14) of the evaluation circuit (37).

5. Method according to Claim 4, characterized in that the comparator component (14) is acted upon by a current V_{CC} (19).

6. Method according to Claim 5, characterized in that the current V_{CC} (19) intrudes on one of the inputs (17, 18) of the comparator comparator (14).

7. Method according to Claim 4, characterized in that the pulse inputs (17, 18) of the comparator component (14) that are detected at the first power semiconductor component (7) are supplied, which comparator component switches over its output (16) when a natural voltage V_{CC} is exceeded.

8. Method according to Claim 7, characterized in that the number of edge changes (20) occurring when switching over the output (16) is supplied to an input (27) of the micro-controller (25).

9. Method according to Claim 8, characterized in that during partial load operation (PWM timing signal < 100%) of the electric drive (3), the number of edge changes (20) A1* detected in the evaluation circuit (37) is compared in the micro-controller (25) with the to-be-expected number of edge changes (20) A1.

10. Method according to Claim 8, characterized in that during full load operation (PWM timing signal = 100%) of the electric drive (3), the PWM signal (29, 30) is cyclically switched to a reduced PWM signal and the number of edge changes (20) A2* detected in the evaluation circuit (37) is compared in the micro-controller (25) with the to-be-expected number of edge changes (20) A2.

11. Method according to Claim 9 or 10, characterized in that when the detected number A1*, A2* of edge changes (20) falls short of the to-be-expected number of edge changes (20) A1, A2, the conclusion can be drawn that there is a defect at the first power semiconductor element (7), at the electric drive (3) in a free-wheeling circuit and the flow of current to the electric drive (3) is halted.

12. Method according to Claim 1, characterized in that the triggering of an electrical drive (3), to which a free-wheeling circuit (6) containing a second power semiconductor component (32) is allocated, takes place via a PWM signal (31), which is output to a first PWM triggering branch (32) and a second PWM triggering branch (34) for alternating triggering of the power semiconductor components (7, 32).

13. Method according to Claim 12, characterized in that the PWM signal (31) is inverted in one of the PWM triggering branches (33, 34).

14. Method according to Claim 2, characterized in that an absolute value of a voltage U_1 is detected at one of the taps (11, 12) allocated to the first power semiconductor component (7) and output to the micro-controller (25) on the input side.

15. Method according to Claim 14, characterized in that a comparison of the detected absolute value of voltage U_1 takes place in the micro-controller (25) to a limit voltage $U_{1, Limit}$ with an adaptation of the limit voltage $U_{1, Limit}$ to the PWM signal (29) and the supply voltage U_B of the voltage source (1).

16. Method according to Claim 1, characterized in that the current flowing at one of the gates (9, 10) of the first power semiconductor component (7) is supplied via a resistor (R_S) to the evaluation circuit (37).